(10/701,497)

AMENDMENTS TO THE SPECIFICATION

IN THE SPECIFICATION:

Page 1:

After the title, insert the following paragraph:

CROSS-REFERENCE TO RELATED APPLICATION

This application is a division of Application No. 10/166,145 filed June 11, 2002.

Page 1:

Please substitute the following paragraph for the paragraph beginning at line 10:

NB 12/7/06

Of electrically programmable nonvolatile semiconductor memory devices, a bulk erasable memory or so-called flash memory is known. Flash memories provide excellent portability and shock ~~proof~~ resistance and are electrically bulk erasable. ~~From~~ For these reasons, demands for flash memories as storage devices of compact portable information apparatuses such as portable personal computers and digital still cameras are rapidly increasing. Reduction in a bit cost by a smaller memory cell area is an important factor for market expansion. Various memory cells realizing this have been proposed, for example, as described in " Ohyo

Butsuri (or Applied Physics)", Vol. 65, No. 11, pp. 1114 - 1124 published by the Japan Society of Applied Physics on November 10, 1996 (hereinafter called "Document 1").

Page 1:

Please substitute the following paragraph for the paragraph beginning at line 24:

NR 12/7/06

A virtual ground type memory cell utilizing a three-layer polysilicon gate is described, for example, in JP-B-2694618 (registered on September 12, 1997) corresponding to U.S. Patent 5,095,344. This memory cell is constituted of semiconductor regions formed in a well of a semiconductor substrate and three gates. The three gates include a control gate formed on the well and an erase gate formed between the control gate and a floating gate disposed near each other. These three gates are made of polysilicon and are separated by insulator films. The floating gate and well are also separated by an insulator film. The control gate extending in the row direction constitutes a word line. The source/drain diffusion regions are formed along the column direction and are of a virtual ground type that shares the diffusion regions with adjacent memory cells. With this layout, a pitch in the row direction can be ~~relaxed~~reduced. The erase gate is parallel to the channel